

**IN THE SPECIFICATION**

Please replace the paragraph beginning on page 2, line 6, with the following rewritten paragraph:

The manufacturing method of semiconductor devices according to the U.S. Patent No. 6,043,537 includes preparing a semiconductor substrate that has a DRAM cell array region and a peripheral circuit region. Active regions are formed at the semiconductor substrates. Word lines and gate electrodes are formed in the DRAM cell array region and the peripheral circuit region, respectively. The word lines are formed to extend across the active regions in the DRAM cell array region, and the gate electrodes are formed to extend across the active regions in the peripheral circuit region. Impurity ions are then implanted into the active regions using the word lines and the gate electrodes as ion implantation masks, thereby forming low concentration source/drain regions. As a result, first and second low concentration source regions as well as a common low concentration drain region are formed at the respective active regions in the DRAM cell array region. The first and second low concentration source regions correspond to storage node junctions of DRAM cells.